Chapter 3

Main Differences in Processing Si and SiC Devices

Fan Li and Mike Jennings

Additional information is available at the end of the chapter

http://dx.doi.org/10.5772/intechopen.76293

Abstract

Due to the different physical properties of Si and SiC, many conventional Si device processing techniques cannot be directly transferred to SiC device fabrication. To deliver high-performance SiC commercial power devices, new techniques quite different from Si industry were developed in past decades for processing device, such as dopant implantation, metal contact, MOS interface, etc. On the other hand, the physics model behind many of these SiC processing technologies is not updated in the same pace that the success of them can still not be fully understood.

Keywords: SiC processing, dopant implantation, metal contact, MOS interface, physics model

1. Introduction

Silicon has dominated the electronics industry ever since it was born. In power electronics area, nearly all commercial power devices are made of Si nowadays. However, due to the target of a more environmental friendly society, there has been a continuously increasing demand of power devices working in more harsh conditions such as higher power, higher temperature, higher frequency or even higher radiation, some of which are well beyond the physical limits of Si. For the first time, the position of Si is challenged by some other materials, most of which have a larger band gap than Si, thus called wide band gap (WBG) semiconductors, including silicon carbide (SiC), gallium nitride (GaN) and diamond. SiC may be the most promising candidate at the moment, whose technology is most mature among WBG semiconductors with commercial devices readily on the market [1, 2], and most importantly, SiC is the only WBG semiconductor with SiO_2 as the nature oxide, which is used extensively in power devices as insulators, dielectrics and diffusion barriers [3]. Just as the SiC substrate and epilayer

growth technologies which had gone through decades of developments before power device quality level wafers can be delivered, SiC device processing techniques were improved as well at the same time. It has been studied intensively in last 20 years, and although there is still plenty of room to be improved, commercial power MOSFETs and Schottky diodes with some more conventional structures are not an issue anymore. This chapter will talk about the state-of-the-art processing techniques for SiC devices, including intentional doping, electrical activation, metal/semiconductor interfaces and MOS interface. Particularity, the difference between Si and SiC processing in these areas will be discussed.

2. Intentional doping in SiC

In 1930, Bernhard Gudden [4] was the first one to report that the electrical carriers of semiconductors are actually the impurities within their crystal lattices. If the impurity concentration is too high, the semiconductor becomes metallic, and if too low, more like an insulator.

2.1. Thermal diffusion and ion implantation

Impurities are usually introduced to the bulk semiconductor in early stages of a device fabrication process. Most commonly used dopants are from group V (N, P and As) for n-type and group III (B, Al and Ga) for p-type doping purposes. Doping a bulk semiconductor can be relative easily achieved by adding dopant elements into the epilayer growing process, and the impurity level can be modulated by controlling the precursor gas concentrations [5]. Take a typical vertical MOSFET structure as an example; on the epilayer surface, specific n-type and p-type regions are required to form ohmic contact, MOS channel and body diode. The selective doping area is usually defined by doping masks made of dielectrics or metals using standard photolithography processes. Nowadays the selective doping of semiconductor is achieved mostly in two ways, namely, thermal diffusion and ion implantation.

It is well known that molecules tend to move from higher to lower concentration regions, and this process can be enhanced by increasing the ambient temperature, pressure or concentration gradient in-between. This idea is adopted in semiconductor industry to introduce impurities using dopant sources with various phases: gas, liquid or solid. Thermal diffusion-based doping process often occurs in a quarts tube (see **Figure 1**) in an inert gas atmosphere to minimise contaminations. The dopants firstly arrived at the semiconductor surface form a relative high impurity concentration region; consequently, a concentration gradient exists between the surface and bulk, after which the diffusion is initiated by the thermal energy provided. With time going on, dopants diffuse deeper into the semiconductor bulk, and when the desired doping profile is obtained, it can be stopped quite conveniently by simply cutting the heat supply.

Attributed to the developments of experimental physics, ion implanting dopants directly into semiconductors are also an option now. Ion implanters were not widely available to device engineers until the 1970s [6], while now it is commonly used in both lab and industry processing. In an ion implantation system, dopants are ionised atoms generated from an ion source

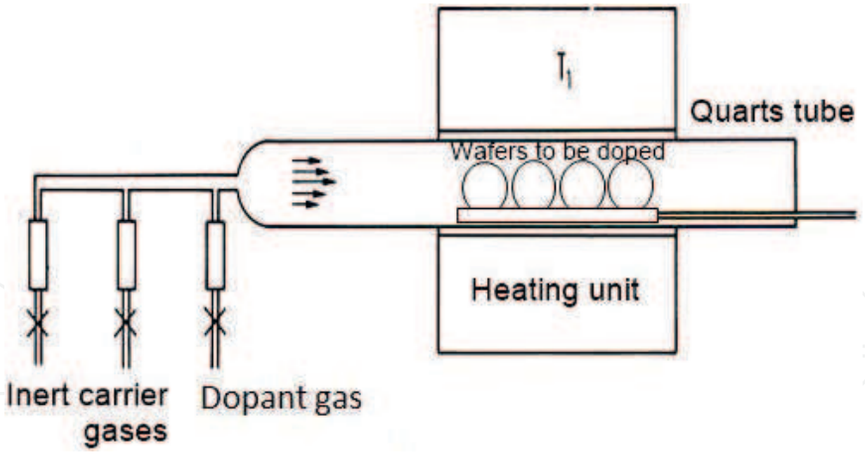

Figure 1. Schematic graph showing a typical dopant thermal diffusion process using a gas source.

shown in **Figure 2**. Being ionised, the dopant atoms can be accelerated by electromagnetic field to gain energy so high that, when hitting the target surface, they are able to break the semiconductor chemical bonds and penetrate into the crystal lattices. The implantation depth can be controlled by changing the electromagnetic field strength, and the resultant impurity concentration (cm^{-3}) is determined by the amount of dopants supplied by the source, which is called 'dose', and the unit is number per specific area (cm^{-2}).

In Si device processing, both thermal diffusion and ion implantation can be used depending on specific requirements. In fact, implantation followed by a short time thermal diffusion is becoming popular nowadays. For WBG semiconductors such as SiC, however, diffusion coefficients of common dopants are so low that are negligible below 1800°C [8], which leaves ion implantation the only option, and the PIA process is essential.

Even being a more complex and expensive system, ion implantation proved to be more controllable than thermal diffusion. Also, the movement of dopants in a thermal diffusion process may involve unexpected spreading in other directions, leading to poor doping profiles. This is not an issue for ion implantation since dopant movement in the semiconductor is minimal, which means the elimination of dopant out-diffusion. There are, of course, also limitations for ion implantations. First of all, it is essentially a dopant bombarding process, which means damages are inevitably induced to the target, mainly in the surface region. Secondly, as-implanted dopants are almost always interstitial (not chemically bonded), namely, not active carriers. An extra post-implantation annealing (PIA) process is typically required to recover the lattice damage and put the implanted dopants into substitutional positions so they can contribute to current conduction, called dopant activation.

2.2. Activating implanted dopants in SiC

The activation of dopants in 4H-SiC has been intensively studied, and the efforts are mainly put into two directions, namely, protecting the semiconductor surface morphology while at the same time maximising the active concentration of implanted dopants.

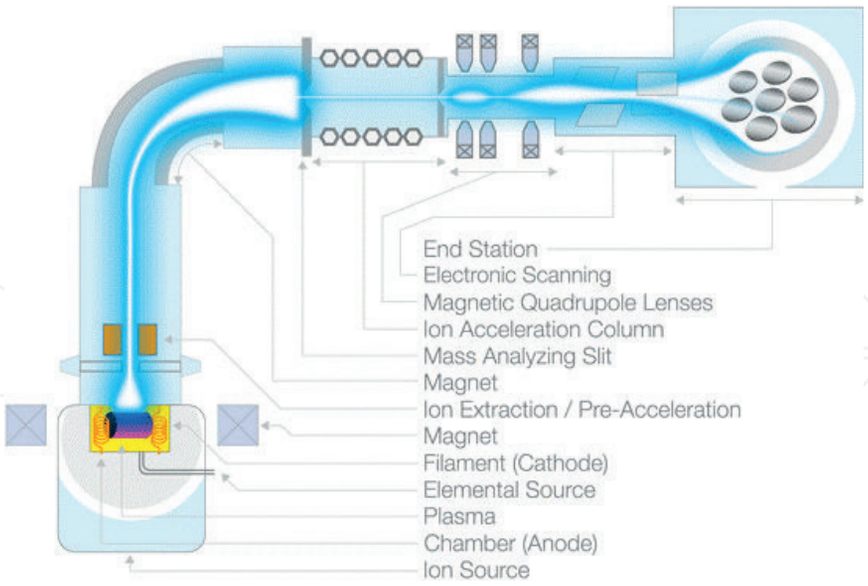

Figure 2. The schematic diagram of an ion implantation system [7].

The temperature required for SiC post-implantation activation (PIA) is very high that above 1400°C [9, 10] is common for n-type and even higher (>1600°C) for p-type [11–13] since acceptors generally sit deeper in the band gap than donors, namely, more difficult to activate. This high temperature means conventional quartz tubes are not up to the task and high melting point tubes made of Al_2O_3 and SiC or similar have to be used. Also, high-temperature annealing leads to a roughened semiconductor surface (known as 'step bunching'), enhanced at implanted regions. This can deteriorate the performance of interface features such as Schottky contacts and FET channels [14–16]. A protection capping layer is often used to preserve the SiC surface; such cap materials studied for 4H-SiC include AlN [17, 18], BN/AlN [19] and graphite [12, 15]. AlN and BN/AlN processes are found complex and expensive, thus not widely accepted. The graphite cap proved to be effective in preserving surface morphology up to 1800°C [11] but may reduce the MOSFET channel mobility due to the excessive silicon vacancies, which are most likely induced by the reaction between diffused Si atoms and the graphite [11, 20]. A SiO_2 layer should not react with Si or C at the common annealing temperatures and can be easily deposited by CVD method and removed via HF etching. It was also studied and resulted a similar surface roughness level as a graphite cap with the same annealing conditions [21]. In the few literatures on 3C-SiC, n-type implanted 3C-SiC was studied for different annealing conditions (1150–1400°C) with [22] and without [23, 24] a graphite cap, and it turned out that there was little advantage of using a graphite cap in terms of protecting the 3C-SiC surface, probably because the temperature limited by Si substrates is not high enough to make the difference.

For a given implanted doping level, the active dopant concentration in SiC generally increases with the PIA temperature. And for a fixed PIA temperature, the active dopant concentration increases with the implanted doping level [25], although the percentage of activated dopants (activation rate) seems to decrease [9]. Complete activation of N-type implanted 4H-SiC has been demonstrated by annealing at 1700°C and using phosphorous as dopant [26], while P-type material still remains a challenge [12].

http://dx.doi.org/10.5772/intechopen.76293

3. Ohmic contact on SiC

Most metals are known as highly electrical and thermal conductive attributed to their delocalised electrons, not to mention the convenient alloying process which helps to form reliable interactions for packaging. Consequently, they are the most widely used material for contact materials in semiconductor industry. Dating back to Braun's discovery in 1874 [27], the study of metal/semiconductor (M-S) interface is almost as old as the semiconductor device itself. A lot of huge efforts were put into exploring the M-S interface, and there had been classic physics models that were well developed. Yet still, this area remains active with new discoveries reported, and novel theories developed continuously. The emergence and adoption of WBG semiconductors raise discussions on new experimental results, and the well-established theories are challenged.

3.1. Metal contact interface: classic theory

It can be seen in **Figure 3** that the work functions of most metals used in electronic industry are quite big compared with Si affinity, that is, an inherent energy barrier exists between metal/Si interfaces, preventing free carrier exchange. And due to a much lower affinity value (except for 3C-SiC), this barrier is only getting higher at a metal/SiC interface, which also explains why Schottky behaviour is typically observed for as-deposited metal contacts on

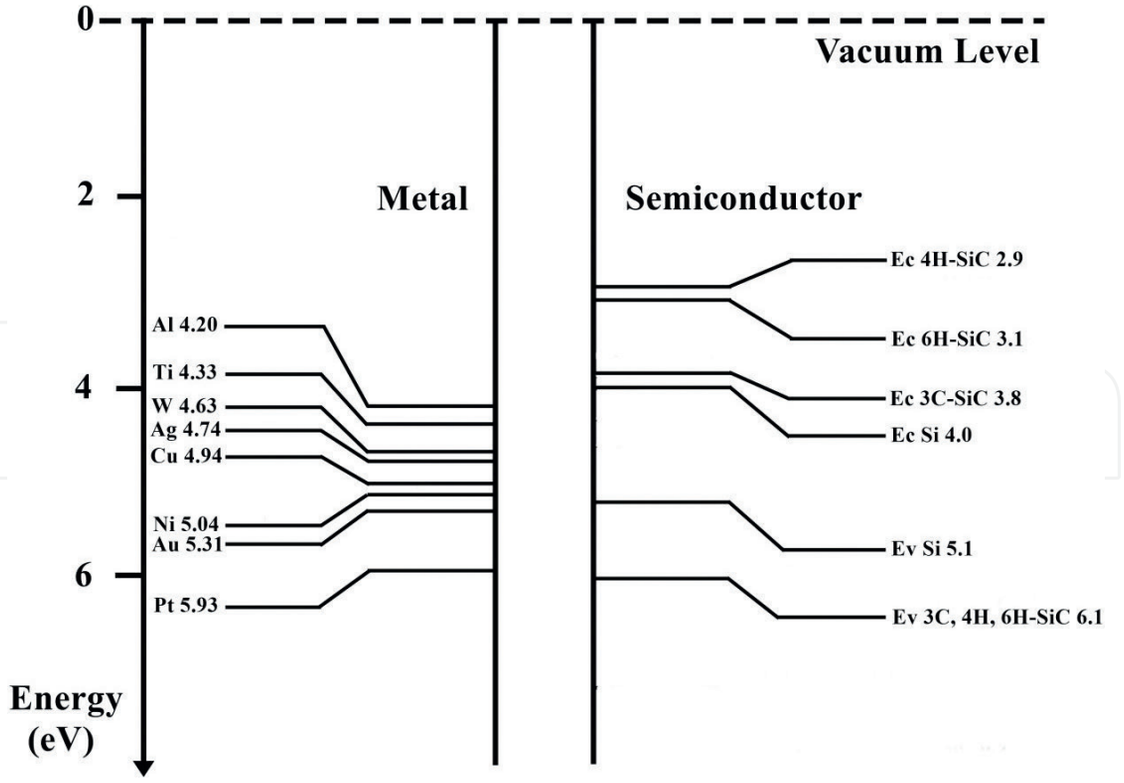

Figure 3. Band diagrams of Si, 3C-, 4H- and 6H-SiC and work functions of commonly used metals in electronic industry [28, 29].

4H-SiC. To fabricate an ohmic contact, increasing the contact region local doping level (via thermal diffusion or ion implantation) is the most common way for both Si and SiC. When the contact region is lowly doped, the depletion region is quite wide that the electron exchange at the M-S interface is only possible when electrons overcome the barrier by gaining enough energy as shown in **Figure 4**, usually thermally activated and thus called thermionic emission (TE). If doping level is very high, the depletion region becomes quite narrow, and electrons can tunnel through the barrier freely with the help of an external electric field, which is called field emission (FE). And if the doping value is in the middle, the depletion region is narrowed but not enough to enable electron tunnelling. In this case, electrons still need extra thermal energy to 'climb up' the barrier, but not as much as TE. The energy required just needs to be adequate for the electrons to 'climb' to a position shallow enough for tunnelling that begins to take effect. Since both TE and FE mechanisms are involved, this is therefore called as thermionic/field emission (TFE).

Among all, FE is the most desired conduction mechanism for deletion-type ohmic contact fabrication, since it is not a thermally activated process, namely, the electrical performance is relative temperature insensitive, which is attractive in more reliable device operation point of view. In real cases, both TFE and FE conduction are quite common. To predict the potential conduction mechanism at the SiC ohmic contact interface, the characteristic energy E_{00} of 3C-, 4H- and 6H-SiC as well as Si is calculated [30] for doping values from 1×10^{16} to 1×10^{20} cm^{-3} and plotted in **Figure 5**. Dielectric constants and electron conductivity effective mass are shown in **Table 1**. The specific boundaries between three mechanisms may vary a bit between groups; the one used in **Figure 5** is proposed by Schroder [31]. As can be seen, to enable FE tunnelling, a doping level above 1×10^{20} cm^{-3} is required for all semiconductors studied here.

Until now, the contact local doping level has been considered as a constant, which cannot be true for WBG materials. This is because with a wider band gap, dopants naturally sit in deeper energy levels and may not be thermally ionised at room temperature; it is called 'freeze-out' [33]. The partial ionisation of carriers leads to quite different ohmic contact performances from conventional theories. Field emission, for example, in which case the contact resistance used

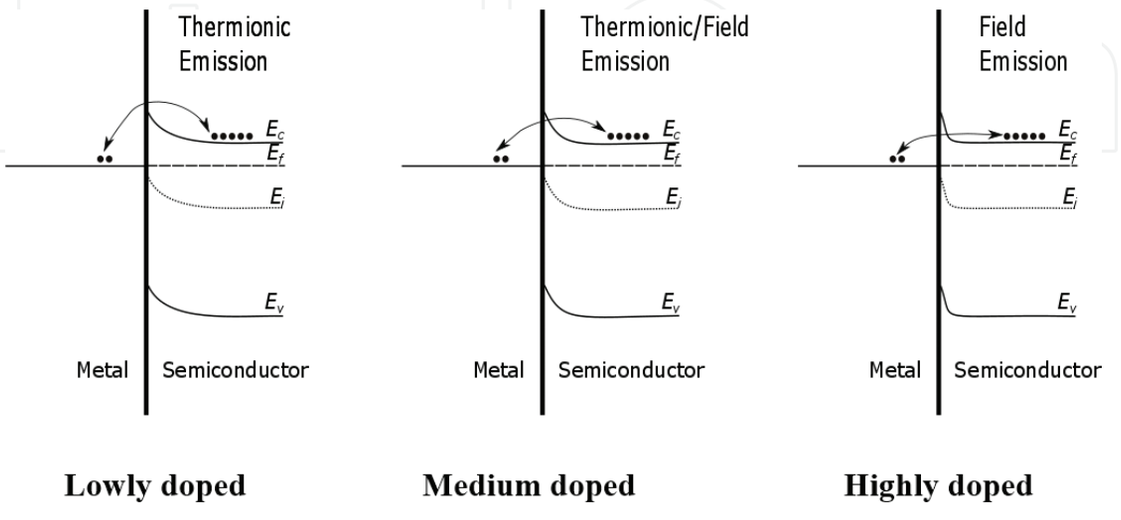

Figure 4. Metal-semiconductor (n-type) interface carrier conduction mechanisms for different doping levels.

http://dx.doi.org/10.5772/intechopen.76293

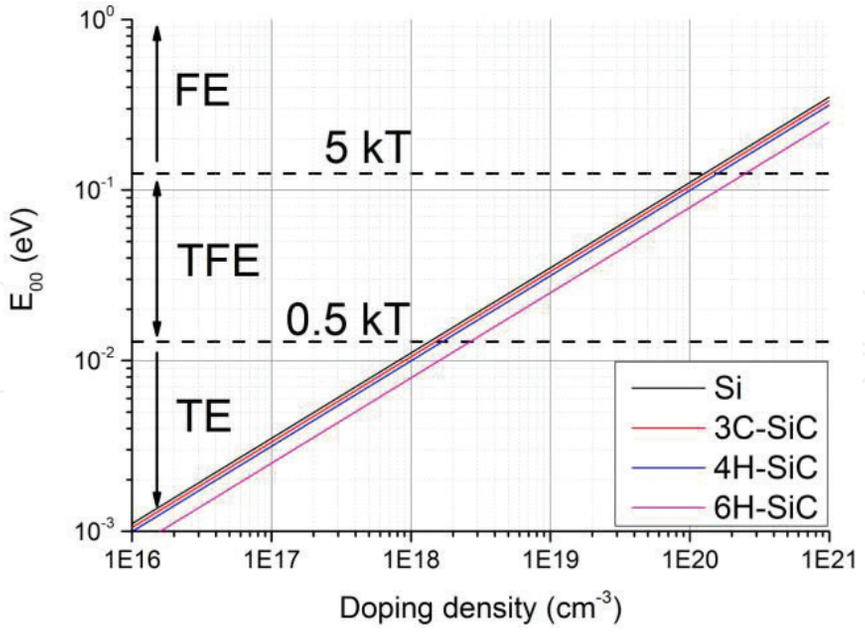

Figure 5. Characteristic energy E_{00} as a function of doping density for n-type Si, 3C-, 4H- and 6H-SiC.

Semiconductor	Dielectric constant	Electron conductivity effective mass
Si	11.7	0.26
3C-SiC	9.72	0.32
4H-SiC	9.66	0.36
6H-SiC	9.66	0.57

Table 1. Dielectric constants and electron conductivity effective mass of Si, 3C-, 4H- and 6H-SiC [32].

to be temperature independent, now will drop with elevating temperature. This is because with more dopants ionised, the contact local doping increases; thus, the depletion width is reduced [34], in favour of the field emission conduction. On the other hand, partial ionisation also means it is more difficult to achieve lower contact resistance at room temperature. To compensate this, after metal deposition on even very highly doped SiC films, extra annealing step (1000–1200°C) is usually required to form a homogeneous silicide or carbide layer at the contact interface, which further lowers the Schottky barrier height, leading to a lower contact resistance. For N-type ohmic contact, nickel-based alloys are typically used, and resultant silicides are Ni_2Si [35], while for P-type, Ti/Al alloys are common, leading to the formation of TiC or Ti_3SiC_2 [36] at the interface after the contact anneal. The complete story behind the rapid thermal anneal for SiC ohmic contact is still not clear; apart from the silicide reaction, which had been consistently observed and confirmed, local carbon clusters [37, 38] enriched at close to the contact interface, potentially providing more free carriers, were also often discussed and may have played a part, too. Specific contact resistance as low as 1×10^{-6} Ω cm^2 [9, 39] can be obtained on N-type SiC ohmic contact, and for the more difficult P-type due to deeper acceptor level, a higher value around 1×10^{-4} Ω cm^2 is typical [12, 36, 40].

4. SiC/SiO_2 MOS interface

Early MOSFETs have a long channel, leading to excessive on-state resistance which is not appropriate for power electronics, thus only applied in low power levels such as microprocessors, microcontrollers and logic circuits. On the other hand, the voltage-control and fast-switching features of MOSFETs are very attractive for power switch applications; consequently many efforts had been put into making power MOSFETs. The first high-voltage structure was developed in the 1970s and called V-MOSFET [41], named after the V-shape grove channel as seen in **Figure 6a**. This design never got popular due to the difficulty in fabricating a smooth V-shape trench on Si substrates, which was at that time formed by potassium hydroxide-based etching, whereas etching rate varies in different crystal orientations [42]. Also, the pointy trench bottom causes severe electric field crowding and easily leads to device early breakdown. Not long after, a planar structure shown in **Figure 6b** was invented. Instead of a V-shape grove, the channel was defined by controlling the thermal diffusion of dopants in the P-base and N^+ source regions, thus called vertical-diffused (VD) MOSFET. With main features relatively easy to fabricate and quite reliable, VD-MOSFET is the most successful design up to date. To achieve higher forward current density, the cell pitch of VD-MOSFET is usually made as small as possible. However, the narrow JFET region between two P-bases restricts the current flowing between channels and drift region, inducing extra on-resistance [43]. In the late 1980s, U-MOSFET design (**Figure 6c**) was proposed as a potential solution of getting rid of the JFET region. U-MOSFET is similar to the V-groove design in the sense that both of them use a trench to eliminate the JFET region, reducing the device on-resistance. By the time U-MOSFET was proposed, Si etching technology had been greatly improved that rounded trench corners are possible with reactive ion etching or other techniques [44]. However, the trench MOS interface and oxide reliability issues are not fully solved; consequently, U-MOSFETs still cannot compete with their planar counterparts.

All three power MOSFET designs introduced above have a vertical structure to maximise current handling ability of discrete devices. For vertical devices, the current rating can be increased by simply enlarging the device active area, such as bigger contacts for diodes or more parallel cells for MOSFETs. In some applications where power devices and control and logic circuits are integrated (e.g. smart power devices, power ICs), the processing and packaging may require all electrodes on the same side of the device, which makes a lateral design necessary, and this is where lateral diffused (LD) MOSFET fits in. As a modification from the long channel design, LDMOSFET usually has a much shorter channel length to minimise the on-resistance. Meanwhile, a long drift region is included for high-voltage purpose as seen in **Figure 6d**. Unlike vertical designs whose breakdown voltage is constrained by the drift region (epilayer) thickness, LDMOSFET utilises the semiconductor surface to greatly increase the device blocking voltage. Inevitably, the current conducting ability of LDMOSFET has to be greatly compromised. As a result, LDMOSFETs are mostly used for RF power amplifiers, microwave and medium power switching applications.

The adoption of WBG semiconductors enables MOSFETs to be used in power electronics applications with much higher power levels. While the Si/SiO_2 interface has been intensively

http://dx.doi.org/10.5772/intechopen.76293

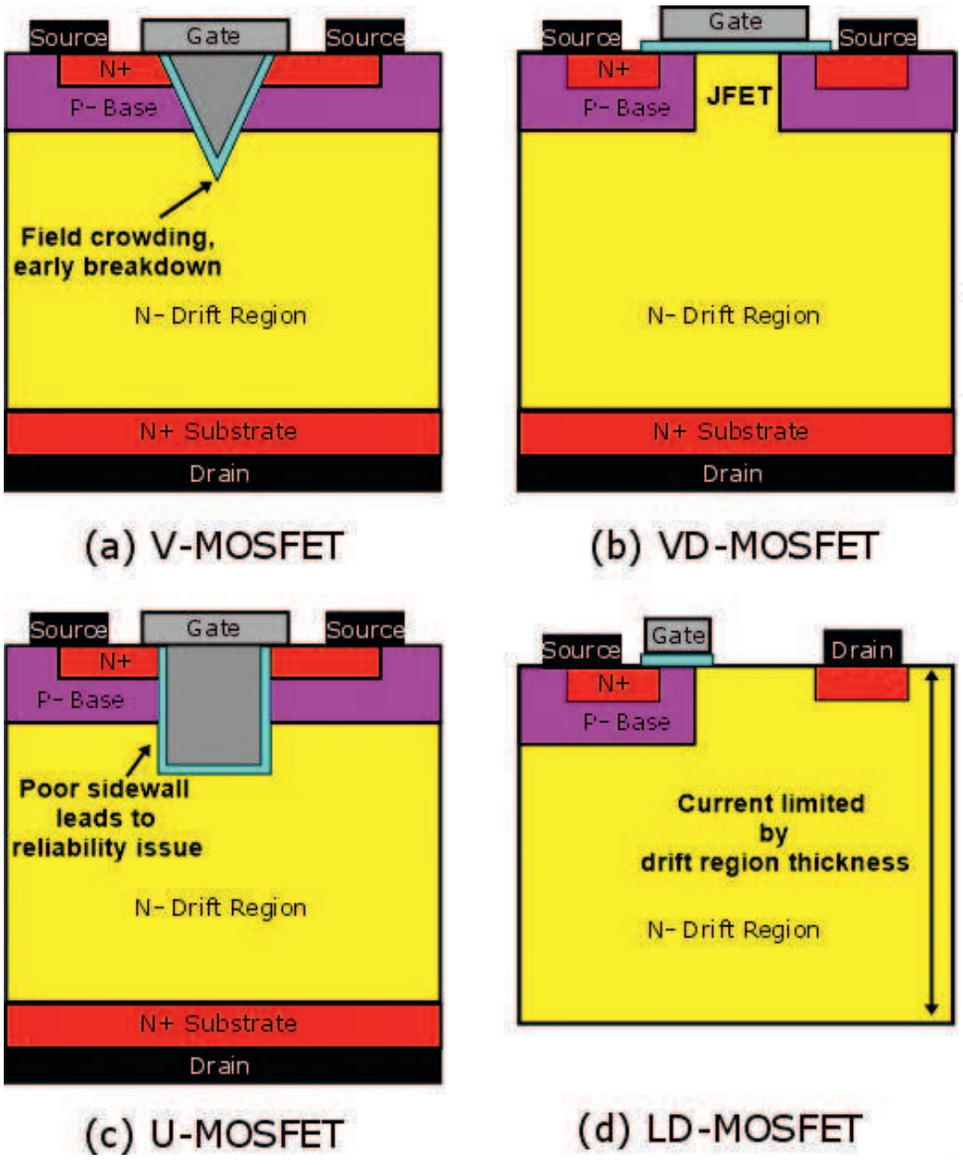

Figure 6. Schematic structure views of various MOSFET designs.

studied and the technology being very mature, the SiC/SiO_2 interface is still an active topic, revealing all kinds of possibilities and challenges.

4.1. Degradation of MOS channel mobility

Apart from phonon and coulombic which also troubles the bulk region, for channel region there is an extra surface roughness scattering mechanism. Among all, the Coulombic scattering caused by extra charges at the MOS interface is more process dependent and has been the target of studies. In real life, gate oxides are often with defects acting as carriers' leakage paths and cause early breakdown. By trapping and discharging carriers during the MOS device operation, these defects (also called states) are the main reason behind the severe Coulombic scattering. Extra charges found in most MOS systems are categorised into four groups, namely,

mobile charges, fixed charges, oxide-trapped charges and interface charges. A schematic graph indicating the general location and polarity of various charges are shown in **Figure 7**.

Mobile charges are metal ionic impurities (such as Na+) introduced during the device fabrication process and can move freely in the oxide with a gate bias. Since positively charged, they will attract semiconductor electrons to the surface and induce extra band bending, leading to a shift of flat band voltage. Mobile charges are highly uncontrollable and thus must be minimised through clean and careful fabrication process. In contrast to mobile charges, fixed charges refer to those who do not move with gate biases. The origin of fixed charges is believed to be the excessive ions left near the interface after the oxidation process termination [45]. They are usually located in the oxide and close to the MOS interface as shown in **Figure 7**. Fixed charges can be both positive and negative, and the total amount depends heavily on the oxidation condition. Since fixed charges stay close to the interface, they also affect the semiconductor band bending. As a result, a shift of flat band voltage from the theoretical value is again observed.

Interface charges, as the name suggests, sit at the MOS interface. Energy levels of these traps are in the semiconductor band gap; consequently, they can act as carrier traps communicating (charge/discharge) with the bulk semiconductor during device operation. And since these traps are right at the MOS interface, they scatter the channel carriers much more than other charges. The origins of interface traps vary among different MOS systems. For Si/SiO_2 interface, most of

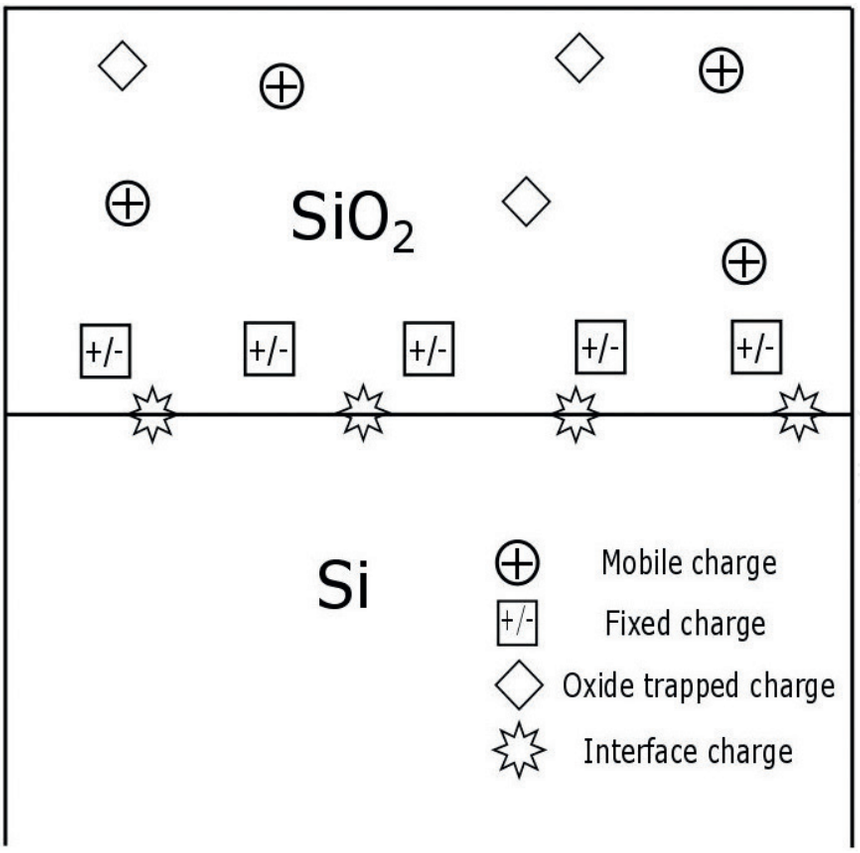

Figure 7. Common oxide charges at MOS interface with locations and charge polarity indicated.

the interface traps come from unterminated Si dangling bonds. H_2 annealing after the gate oxidation is typically applied to passivate the unterminated Si dangling bonds. Unlike the previous three, oxide-trapped charges are induced by the device operation rather than the fabrication process. The oxide layer, thermally grown or deposited, contains intrinsic defects such as oxygen vacancies [46]. Although these defects are electrically neutral, during the device operation, carriers may be injected into them and make them negatively or positively charged. Depending on the energy level, they may or may not be able to communicate with the semiconductor carriers. For those very close to the MOS interface that are able to be charged and discharged during device operation, they effectively behave as interface traps, otherwise similar to fixed charges.

4.2. SiC/SiO_2 interface traps

With all the superior electrical performance and the ability to be thermally oxidised, it is no surprise that there are a lot of interests in making SiC MOS devices. The most commercialised 4H-SiC is naturally mostly studied. The hexagonal lattice of 4H-SiC means there will be several faces available for oxidation. Most of the work has been devoted into the (0001) Si-face, the only one available in commercial wafer form. Following discussions are therefore mainly based on (0001) Si-face. There have been studies suggesting that MOS interface traps for all SiC polytypes are similar [47]; thus, the study on the 4H-SiC/SiO_2 interface also provides a great insight for other polytypes. Unfortunately, the 4H-SiC/SiO_2 interface turns out to be quite poor, and the electrical performance is not even close to the Si case. The interface trap density (D_{it}) at an as-grown 4H-SiC/SiO_2 interface is typically close to 10^{13} cm^{-2} eV^{-1}, which is hundreds of times higher than the Si/SiO_2 interface [48]. The channel mobility generally decreases with increasing D_{it}; thus, the latter is commonly used as an indicator for the MOS interface quality. With decades of study, reasons behind the poor 4H-SiC/SiO_2 interface are still not fully understood. In [46], a discussion was made on the potential origins of interface traps, and two sources were identified, first of which is the carbon accumulated at the MOS interface during the SiC oxidation process. The reactions occurring during Si and SiC oxidation processes can be generally expressed by reactions described in Eqs. (1) and (2):

$$Si(s) + O_2(g) \rightarrow SiO_2(s) \tag{1}$$

$$SiC(s) + x\,O_2(g) \rightarrow SiO_2(s) + CO/CO_2(g) \tag{2}$$

Depending on the oxygen pressure, there may be some intermediate reactions [49], but it can be seen that SiC oxidation is accompanied by the release of gaseous carbon, either CO or CO_2. However, the increase of oxide thickness after the oxidation process goes for a while makes it more difficult for carbon to escape, and the reaction (Eq. (3)) may occur instead:

$$SiC(s) + O_2(g) \rightarrow SiO_2(s) + C(s) \tag{3}$$

The theory of carbon failing to escape through thicker oxide naturally leads to the idea that there should be less carbon at the MOS interface with thinner oxide. Indeed, a recent study [50] demonstrated an almost ideal SiC/SiO_2 interface with a very thin oxide layer (≈14 nm);

the D_{it} value was below 10^{11} cm^{-2} eV^{-1}. However, as mentioned before a certain oxide thickness (≈50 nm for SiC MOS devices) is necessary for a reasonable threshold voltage, which means very thin oxide is not practical in real device fabrications. Thin thermally grown oxide with deposited oxide on top of it may be an option but still not easy, since deposited oxide is known to contain many more defects than thermally grown ones [51].

This leads to the second source of SiC/SiO_2 interface traps, namely, oxide defects. Oxide defect-induced traps are essentially the oxide-trapped charges mentioned before. In SiC/SiO_2 study they are also known as 'near-interface traps' since they do not actually sit at the interface but instead are located in the SiO_2 very close to the interface. For Si, energy levels of oxide-trapped states are in the conduction band, thus not electrically active. For SiC, however, whose band gaps are 2–3 times wider, many of the oxide-trapped charges located in the band gap are being electrically active, as has been confirmed by photon-stimulated electron tunnelling [52]. The near-interface traps have time constants much smaller than the carbon clusters, which are also called fast traps while the latter known as slow traps. A schematic representation of the carbon cluster mode is illustrated in **Figure 8** with energy levels of the traps specified. Due to the much lower mobility of holes than electrons, SiC MOS devices are almost exclusively based on n-channel design; naturally, the traps scattering the channel carriers most are the ones located close to the conduction band edge. **Figure 8** shows that the 4H-SiC conduction band edge is mostly troubled by near-interface traps and π-bonded carbon clusters, with the former more dominant. Both of these traps are accepter-like, namely, negatively charged when being occupied, which can explain the quite positive threshold values often observed for 4H-SiC MOS devices. On the other hand, 3C-SiC is free from near-interface traps attributed to a smaller band gap but is still troubled by π-bonded carbon clusters. These carbon

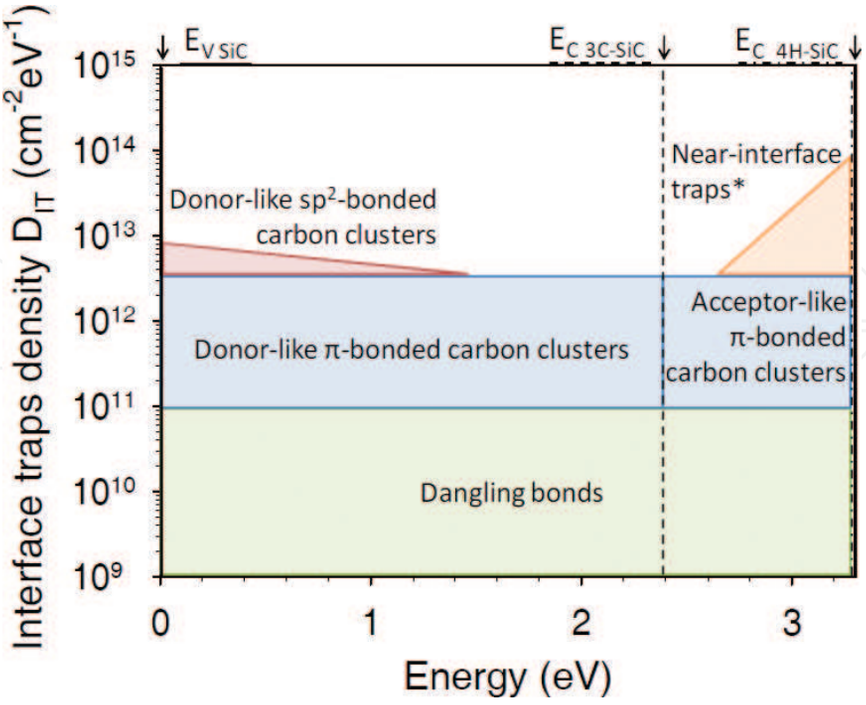

Figure 8. Schematic representation of the 'carbon cluster model' [53].

clusters near the 3C-SiC conduction band edge are donor-like, thus positively charged if unoccupied, which means the resultant threshold voltage may be more negative. Dangling bonds still contribute to some of the interface traps here but are only secondary concerns. Consequently, for SiC, H_2 annealing is not as effective as it is for Si. Other techniques had to be explored for SiC/SiO_2 interface optimisation.

4.3. SiC/SiO_2 interface treatments

The efforts put into improving the SiC/SiO_2 interface can be grouped into three directions, namely, post-oxidation annealing (POA), channel counter-doping and high-temperature oxidation.

Nitridation may be the most widely used method to improve the $4H\text{-}SiC/SiO_2$ interfaces. It is usually achieved by annealing thermally grown gate oxides in nitrogenous trace gas environment (NO or N_2O), called post-oxidation annealing (POA). It is believed that the N-O bond breaks at high temperature and supplies free oxygen which oxidises 4H-SiC [54]; consequently, nitridation by POA is accompanied by a further growth of the oxide, although not significantly. Gate oxide can also be directly grown in such atmosphere to obtain similar benefits. Previous X-ray photoelectron spectroscopy (XPS) results showed that after NO/N_2O POA, there were fixed nitrogen atoms near the interface with a density $\approx 1 \times 10^{14}$ cm^{-2} [55], even after removing all the oxide by a hard HF etching, indicating that nitrogen atoms were strongly bonded to 4H-SiC substrate. There had been evidence showing the nitridation reduced both carbon-related and near-interface traps [56], even though there is still no complete explanation of the theory established. The near-interface traps are probably reduced by the formation of an oxynitride layer between 4H-SiC and gate oxide, which redefines the oxide/semiconductor boundary [57], and the oxide-trapped charges are no longer near the interface. In terms of the carbon clusters, they are probably decomposed by inserted nitrogen atoms, which shift the energy levels of remaining clusters deeper into band gap, namely, further away from the conduction band edge and less effective in terms of scattering channel carriers [58]. Apart from N_2O/NO, it was reported that annealing the gate oxide in a phosphorous trace atmosphere ($POCl_3$ [59] or P_2O_5 [60]) also led to a channel mobility improvement, although it introduced severe threshold voltage instability as a result of SiO_2 being converted into phosphor silicate glasses. Reducing the number of interface traps by introducing extra atoms into the interface is called passivation, and regardless of the source (N or P), it is always required that enough foreign atoms diffuse through the gate oxide and reach the interface. Certainly higher annealing temperature and time duration will help with that; however, due to the very low diffusion coefficient of nitrogen in SiC, nitrogen atoms saturate only within a monolayer deeper into the interface [61], and consequently the mobility value does not increase further, and the peak value typically stays around 40 $cm^2/V\ s$ [62]. Phosphorous has a higher saturation density than nitrogen in 4H-SiC, but still, the peak mobility value stays around 80 $cm^2/V\ s$ [63] regardless of further increased annealing time durations.

The limitation of thermal diffusion naturally leads to the idea of incorporating more passivating atoms into the interface by ion implantation, also known as channel counter-doping. 4H-SiC MOSFETs were fabricated on nitrogen-implanted substrates and higher peak channel mobility

(≈60 $cm^2/V\,s$) than unimplanted or even NO/N_2O annealed samples was observed [64–66], before the mobility curve becomes significantly distorted for a dose level of 2.2×10^{14} cm^{-2}. The success of counter-doping technique brings in another possible explanation [66] other than the defect passivation for the improved 4H-SiC/SiO_2 interface. With the channel surface being partially compensated by the nitrogen implantation, a depletion region is formed between the thin counter-doped n-type surface and the underlying p-type channel region. The n-type counter-doped surface may be positively charged even without any gate bias due to the p-n junction depletion. In inversion mode, higher carrier mobility can be achieved since these positive charges will cancel part of the negative electric field built in the channel region, reducing the surface roughness scattering. Apart from nitrogen, other elements were also studied for the counter-doping. In [67], a variety of ions including B, N, F, Al, P and Cl were individually implanted into a 4H-SiC substrate, which was then oxidised to make MOS capacitors. It turned out only group V elements (N and P) led to a reduced D_{it} while the other increased it. A negative shift of flat band voltage is always observed for N or P counter-doped MOSFETs, a natural result of the channel being partially compensated. For devices fabricated with N- or P-based POAs, similar negative shifts were also observed, which suggests that counter-doping may have occurred in POAs through minor thermal diffusion, making it difficult to distinguish the effects from passivation and counter-doping. More recently [68], counter-doping 4H-SiC MOSFET channel using Sb was studied, and a peak field-effect mobility as high as 80 $cm^2/V\,s$ was obtained. The fact that the mobility value dropped to almost zero at 70 K (Sb freezes out) confirmed that the improvement is not achieved by defect passivation, since otherwise the mobility should only be influenced by SiC electrons and the Sb freeze-out will have minimal effect. Further processing the Sb counter-doped sample with NO POA led to an increased channel mobility in all temperatures including 70 K, which suggests that the counter-doping and defect passivation may be two independent mechanisms, yet both increase the channel mobility.

Both previous methods introduce extra foreign element atoms to the SiC/SiO_2 system. It will be ideal to have an as-oxidised MOS interface free from excessive interface traps. High-temperature oxidation is considered as a possible solution. It was firstly reported in [69] that D_{it} decreases with increasing oxidation temperature, which was related to a reduction of SiC_xO_y near the interface at higher oxidation temperature. More recently [70], a channel mobility of 40 $cm^2/V\,s$ was reported for 4H-SiC MOSFET with gate oxide thermally grown at 1500°C without any further treatment, and the XPS measurement suggests a reduction of carbon near the interface. The mechanism behind high-temperature oxidation is still unclear and needs to be explored more.

Author details

Fan Li[1]* and Mike Jennings[2]

Address all correspondence to: f.li.3@warwick.ac.uk

1 University of Warwick, Coventry, United Kingdom

2 School of Engineering, University of Warwick, Coventry, United Kingdom

References

[1] CoolSiC™ MOSFET, revolution to rely on. Infineon Technologies AG; 2016

[2] Cree redefines the discrete power MOSFET landscape with the industry's first 900-V SiC MOSFET. Cree Press Release; 2015

[3] Dhar S, Song YW, Feldman LC, Isaacs-Smith T, Tin CC, Williams JR, et al. Effect of nitric oxide annealing on the interface trap density near the conduction band edge of 4H--SiC at the oxide/(112-0) 4H--SiC interface. Applied Physics Letters. 2004;**84**:1498-1500. DOI: 10.1063/1.1651325

[4] Busch G. Early history of the physics and chemistry of semiconductors-from doubts to fact in a hundred years. European Journal of Physics. 1989;**10**(4):254-260. DOI: 10.1088/0143-0807/10/4/002

[5] Wijesundara M, Azevedo R. Silicon Carbide Microsystems for Harsh Environments. New York: Springer-Verlag, Springer Science & Business Media; 2011. DOI: 10.1007/978-1-4419-7121-0

[6] Fair RB. History of some early developments in ion-implantation technology leading to silicon transistor manufacturing. Proceedings of the IEEE. 1998;**86**(1):111-137. DOI: 10.1109/5.658764

[7] Group TP. Components and spare parts for ion implantation [Internet]. 2018. Available from: https://www.plansee.com/en/products/components/spare-parts-for-ion implantation.html. [Accessed: 2018-01-02]

[8] Zhe CF. Silicon Carbide: Materials, Processing & Devices. Amsterdam: Taylor & Francis Books, Gordon and Breach Science Pub.; 2004

[9] Li M, Ahyi AC, Zhu X, Chen Z, Isaacs-Smith T, Williams JR, et al. Nickel ohmic contacts to N-implanted (0001) 4H-SiC. Journal of Electronic Materials. 2010;**39**(5):540-544. DOI: 10.1007/s11664-010-1128-1

[10] Vivona M, Greco G, Giannazzo F, Nigro RL, Rascuna S, Saggio M, Roccaforte F. Thermal stability of the current transport mechanisms in Ni-based ohmic contacts on n- and p-implanted 4H-SiC. Semiconductor Science and Technology. 2014;**29**(7):075018. DOI: 10.1088/0268-1242/29/7/075018

[11] Jones KA, Wood MC, Zheleva TS, Kirchner KW, Derenge MA, Bolonikov A, et al. Structural and chemical comparison of graphite and BN/AlN caps used for annealing ion implanted SiC. Journal of Electronic Materials. 2008;**37**(6):917-924. DOI: 10.1007/s11664-008-0405-8

[12] Frazzetto A, Giannazzo F, Nigro RL, Raineri V, Roccaforte F. Structural and transport properties in alloyed Ti/Al Ohmic contacts formed on p-type Al-implanted 4H-SiC annealed at high temperature. Journal of Physics D: Applied Physics. 2011;**44**(25):255302. DOI: 10.1088/0022-3727/44/25/255302

[13] Jacob C, Pirouz P, Kuo HI, Mehregany M. High temperature ohmic contacts to 3C–silicon carbide films. Solid-State Electronics. 1998;**42**(12):2329-2334. DOI: 10.1016/S0038-1101(98)00234-2

[14] Capano MA, Ryu S, Cooper JA Jr, Melloch MR, Rottner K, Karlsson S, et al. Surface roughening in ion implanted 4H-silicon carbide. Journal of Electronic Materials. 1999; **28**(3):214-218. DOI: 10.1007/s11664-999-0016-z

[15] Negoro Y, Katsumoto K, Kimoto T, Matsunami H. Electronic behaviors of high-dose phosphorus-ion implanted 4H–SiC (0001). Journal of Applied Physics. 2004;**96**(1):224-228. DOI: 10.1063/1.1756213

[16] Vassilevski KV, Wright NG, Nikitina IP, Horsfall AB, O'Neill AG, Uren MJ, Hilton KP, Masterton AG, Hydes AJ, Johnson CM. Protection of selectively implanted and patterned silicon carbide surfaces with graphite capping layer during post-implantation annealing. Semiconductor Science and Technology. 2005;**20**(3):271-278. DOI: 10.1088/0268-1242/20/3/003/meta

[17] Derenge MA, Jones KA, Kirchner K, Ervin M, editors. A Comparison of the AlN Annealing Cap for 4H SiC Annealed in a Nitrogen Versus an Argon Atmosphere. 2003 International Semiconductor Device Research Symposium; 2003. DOI: 10.1109/ISDRS.2003.1272026

[18] Jones KA, Shah PB, Kirchner KW, Lareau RT, Wood MC, Ervin MH, et al. Annealing ion implanted SiC with an AlN cap. Materials Science and Engineering: B. 1999;**61-62**:281-286. DOI: 10.1016/S0921-5107(98)00518-2

[19] Ruppalt L, Stafford S, Yuan D, Vispute R, Venkatesan T, Sharma R, et al. Using a PLD BN/AlN composite as an annealing cap for ion implanted SiC. In: 2001 International Semiconductor Device Research symposium; 2001. DOI: 10.1109/ISDRS.2001.984565

[20] Naik H, Tang K, Chow TP. Effect of graphite cap for implant activation on inversion channel mobility in 4H-SiC MOSFETs. Materials Science Forum. 2009;**615-617**:773-776. DOI: 10.4028/www.scientific.net/MSF.615-617.773

[21] Zhao F, Islam MM, Huang C-F. Study of SiO_2 encapsulation for aluminium and phosphorus implant activation in 4H-SiC. Materials Letters. 2010;**64**(23):2593-2596. DOI: 10.1016/j.matlet.2010.08.048

[22] Song X, Biscarrat J, Michaud J-F, Cayrel F, Zielinski M, Chassagne T, et al. Structural and electrical characterizations of n-type implanted layers and ohmic contacts on 3C-SiC. Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms. 2011;**269**(18):2020-2025. DOI: 10.1016/j.nimb.2011.06.004

[23] Bazin A, Michaud J, Autret-Lambert C, Cayrel F, Chassagne T, Portail M, et al. Ti–Ni ohmic contacts on 3C–SiC doped by nitrogen or phosphorus implantation. Materials Science and Engineering: B. 2010;**171**(1):120-126. DOI: 10.1016/j.mseb.2010.03.084

[24] Song X, Bazin AE, Michaud JF, Cayrel F, Zielinski M, Portail M, et al. Electrical characterization of nitrogen implanted 3C-SiC by SSRM and CTLM measurements. Materials Science Forum. 2011;679**-680**:193-196. DOI: 10.4028/www.scientific.net/MSF.679-680.193

[25] Parisini A, Gorni M, Nath A, Belsito L, Rao MV, Nipoti R. Remarks on the room temperature impurity band conduction in heavily Al+ implanted 4H-SiC. Journal of Applied Physics. 2015;**118**(3):035101. DOI: 10.1063/1.4926751

[26] Laube M, Schmid F, Pensl G, Wagner G, Linnarsson M, Maier M. Electrical activation of high concentrations of N+ and P+ ions implanted into 4H–SiC. Journal of Applied Physics. 2002;**92**(1):549-554. DOI: 10.1063/1.1479462

[27] Braun F. On the current transport in metal sulfides. Annual Review of Physical Chemistry. 1874;**153**:556-563

[28] Lide D, Bruno TJ, Haynes W. CRC Handbook of Chemistry and Physics: A Ready-Reference Book of Chemical and Physical Data. Boca Raton: CRC Press; 2009

[29] Roccaforte F, Giannazzo F, Raineri V. Nanoscale transport properties at silicon carbide interfaces. Journal of Physics D: Applied Physics. 2010;**43**(22):223001. DOI: 10.1088/0022-3727/43/22/223001/meta

[30] Padovani FA, Stratton R. Field and thermionic-field emission in Schottky barriers. Solid-State Electronics. 1966;**9**(7):695-707. DOI: 10.1016/0038-1101(66)90097-9

[31] Schroder DK. Semiconductor Material and Device Characterization. 3rd ed. Hoboken, New Jersey: John Wiley & Sons; 2006. DOI: 10.1002/0471749095

[32] Levinshtein ME, Rumyantsev SL, Shur MS. Properties of Advanced Semiconductor Materials: GaN, AIN, InN, BN, SiC, SiGe. New York, Chichester, Weinheim, Brisbane, Singapore, Toronto: John Wiley & Sons; 2001

[33] Shou-Guo W, Yi-Men Z, Yu-Ming Z. Theoretical investigation of incomplete ionization of dopants in uniform and ion-implanted 4H-SiC MESFETs. Chinese Physics. 2003;**12**(1):89-93. DOI: 10.1088/1009-1963/12/1/316

[34] Perez-Tomas A, Fontsere A, Placidi M, Jennings MR, Gammon PM. Modelling the metal–semiconductor band structure in implanted ohmic contacts to GaN and SiC. Modelling and Simulation in Materials Science and Engineering. 2013;**21**(3):035004. DOI: 10.1088/0965-0393/21/3/035004/meta

[35] Kuchuk A, Kladko V, Guziewicz M, Piotrowska A, Minikayev R, Stonert A, Ratajczak R. Fabrication and characterization of nickel silicide ohmic contacts to n-type 4H silicon carbide. Journal of Physics: Conference Series. 2008;**100**(4):042003. DOI: 10.1088/1742-6596/100/4/042003/meta

[36] Jennings MR, Fisher CA, Walker D, Sanchez A, Pérez-Tomás A, Hamilton DP, et al. On the Ti_3SiC_2 metallic phase formation for robust p-Type 4H-SiC ohmic contacts. Materials Science Forum. 2014;**778-780**:693-696. DOI: 10.4028/www.scientific.net/MSF.778-780.693

[37] Levit M, Grimberg I, Weiss BZ. Interaction of Ni90Ti10 alloy thin film with 6H-SiC single crystal. Journal of Applied Physics. 1996;**80**(1):167-173. DOI: 10.1063/1.362801

[38] Roccaforte F, La Via F, Baeri A, Raineri V, Calcagno L, Mangano F. Structural and electrical properties of Ni/Ti Schottky contacts on silicon carbide upon thermal annealing. Journal of Applied Physics. 2004;**96**(8):4313-4318. DOI: 10.1063/1.1787138

[39] Biscarrat J, Song X, Michaud JF, Cayrel F, Portail M, Zielinski M, et al. Ti thickness influence for Ti/Ni ohmic contacts on n-type 3C-SiC. Materials Science Forum. 2012;**711**:179-183. DOI: 10.4028/www.scientific.net/MSF.711.179

[40] Fisher C, Jennings M, Sharma Y, Sanchez-Fuentes A, Walker D, Gammon P, et al. On the Schottky barrier height lowering effect of Ti_3SiC_2 in ohmic contacts to P-Type 4H-SiC. International Journal of Fundamental Physical Sciences. 2014;**4**(3). DOI: 10.14331/ijfps.2014.330071

[41] Holmes FE, Salama CAT. VMOS—A new MOS integrated circuit technology. Solid-State Electronics. 1974;**17**(8):791-797. DOI: 10.1016/0038-1101(74)90026-4

[42] Baliga BJ. Fundamentals of Power Semiconductor Devices. Springer Science & Business Media; 2010. DOI: 10.1007/978-0-387-47314-7_6

[43] Ng JCW, Sin JKO. A low-voltage planar power MOSFET with a segmented JFET region. IEEE Transactions on Electron Devices. 2009;**56**(8):1761-1766. DOI: 10.1109/TED.2009.2024105

[44] Saxena RS, Kumar MJ. Trench gate power MOSFET: Recent advances and innovations. In: Jit S, editor. Advances in Microelectronics and Photonics, Chapter 1. NY: Nova Science Publishers Inc; 2012. pp. 1-23

[45] Brennan KF. Introduction to Semiconductor Devices: For Computing and Telecommunications Applications. New York: Cambridge University Press; 2005

[46] Afanasev VV, Bassler M, Pensl G, Schulz M. Intrinsic SiC/SiO_2 interface states. Physica Status Solidi (a). 1997;**162**(1):321-337. DOI: 10.1002/1521-396X(199707)162:1<321::AID-PSSA321>3.0.CO;2-F

[47] Afanasev VV, Ciobanu F, Pensl G, Stesmans A. Contributions to the density of interface states in SiC MOS structures. In: Choyke WJ, Matsunami H, Pensl G, editors. Silicon Carbide: Recent Major Advances. Verlag, Berlin, Heidelberg and New York: Springer; 2004. pp. 343-371. DOI : 10.1007/978-3-642-18870-1

[48] Liu G, Tuttle BR, Dhar S. Silicon carbide: A unique platform for metal-oxide-semiconductor physics. Applied Physics Reviews. 2015;**2**(2):021307. DOI: 10.1063/1.4922748

[49] Roy J, Chandra S, Das S, Maitra S. Oxidation behaviour of silicon carbide-a review. Review on Advanced Materials Science. 2014;**38**:29-39

[50] Kikuchi RH, Kita K. Fabrication of SiO_2/4H-SiC (0001) interface with nearly ideal capacitance-voltage characteristics by thermal oxidation. Applied Physics Letters. 2014;**105**(3):032106. DOI: 10.1063/1.4891166

[51] Viana CE, Silva ANRd, Morimoto NI, Bonnaud O. Analysis of SiO_2 thin films deposited by PECVD using an oxygen-TEOS-argon mixture. Brazilian Journal of Physics. 2001;**31**:299-303. DOI: 10.1590/S0103-97332001000200023

[52] Afanas'ev VV, Stesmans A. Photon-stimulated tunnelling of electrons in SiO_2: Evidence for a defect-assisted process. Journal of Physics: Condensed Matter. 1997;**9**(6):L55. DOI: 10.1088/0953-8984/9/6/002

[53] Esteve R. Fabrication and Characterization of 3C-and 4H-SiC MOSFETs [thesis]. School of Information and Communication Technology (ICT), KTH; 2011.

[54] Morales-Acevedo A, Santana G, Carrillo-López J. Thermal oxidation of silicon in nitrous oxide at high pressures. Journal of The Electrochemical Society. 2001;**148**(10):F200-F202. DOI: 10.1149/1.1398278

[55] Kosugi R, Umeda T, Sakuma Y. Fixed nitrogen atoms in the SiO_2/SiC interface region and their direct relationship to interface trap density. Applied Physics Letters. 2011;**99**(18): 182111. DOI: 10.1063/1.3659689

[56] Afanas'ev VV, Stesmans A, Ciobanu F, Pensl G, Cheong KY, Dimitrijev S. Mechanisms responsible for improvement of 4H–SiC/SiO_2 interface properties by nitridation. Applied Physics Letters. 2003;**82**(4):568-570. DOI: 10.1063/1.1532103

[57] Rozen J, Dhar S, Zvanut ME, Williams JR, Feldman LC. Density of interface states, electron traps, and hole traps as a function of the nitrogen density in SiO_2 on SiC. Journal of Applied Physics. 2009;**105**(12):124506. DOI: 10.1063/1.3131845

[58] McDonald K, Weller RA, Pantelides ST, Feldman LC, Chung GY, Tin CC, et al. Characterization and modelling of the nitrogen passivation of interface traps in SiO_2/4H–SiC. Journal of Applied Physics. 2003;**93**(5):2719-2722. DOI: 10.1063/1.1542935

[59] Okamoto D, Yano H, Kenji H, Hatayama T, Fuyuki T. Improved inversion channel mobility in 4H-SiC MOSFETs on Si face utilizing phosphorus-doped gate oxide. Electron Device Letters, IEEE. 2010;**31**(7):710-712. DOI: 10.1109/LED.2010.2047239

[60] Sharma YK, Ahyi AC, Isaacs-Smith T, Modic A, Park M, Xu Y, et al. High-mobility stable 4H-SiC MOSFETs using a thin PSG interfacial passivation layer. Electron Device Letters, IEEE. 2013;**34**(2):175-177. DOI: 10.1109/LED.2012.2232900

[61] Chen Z, Xu Y, Garfunkel E, Feldman LC, Buyuklimanli T, Ou W, et al. Kinetics of nitrogen incorporation at the SiO_2/4H-SiC interface during an NO passivation. Applied Surface Science. 2014;**317**:593-597. DOI: 10.1016/j.apsusc.2014.08.181

[62] Rozen J, Ahyi AC, Xingguang Z, Williams JR, Feldman LC. Scaling between channel mobility and interface state density in SiC MOSFETs. IEEE Transactions on Electron Devices. 2011;**58**(11):3808-3811. DOI: 10.1109/TED.2011.2164800

[63] Sharma YK, Ahyi AC, Issacs-Smith T, Shen X, Pantelides ST, Zhu X, et al. Phosphorous passivation of the SiO_2/4H–SiC interface. Solid-State Electronics. 2012;**68**:103-107. DOI: 10.1016/j.sse.2011.10.030

[64] Moscatelli F, Poggi A, Solmi S, Nipoti R. Nitrogen implantation to improve electron channel mobility in 4H-SiC MOSFET. IEEE Transactions on Electron Devices. 2008;**55**(4):961-967. DOI: 10.1109/TED.2008.917107

[65] Poggi A, Moscatelli F, Hijikata Y, Solmi S, Nipoti R. MOS capacitors obtained by wet oxidation of n-type 4H–SiC pre-implanted with nitrogen. Microelectronic Engineering. 2007;**84**(12):2804-2809. DOI: 10.1016/j.mee.2007.01.241

[66] Dhar S, Sei-Hyung R, Agarwal AK. A study on pre-oxidation nitrogen implantation for the improvement of channel mobility in 4H-SiC MOSFETs. IEEE Transactions on Electron Devices. 2010;**57**(6):1195-1200. DOI: 10.1109/TED.2010.2045670

[67] Okamoto D, Yano H, Hatayama T, Fuyuki T. Systematic investigation of interface properties in 4H-SiC MOS structures prepared by over-oxidation of ion-implanted substrates. Materials Science Forum. 2010;**645-648**:495-498. DOI: 10.4028/www.scientific.net/MSF.645-648.495

[68] Modic A, Gang L, Ahyi AC, Yuming Z, Pingye X, Hamilton MC, et al. High channel mobility 4H-SiC MOSFETs by antimony counter-doping. Electron Device Letters. 2014;**35**(9): 894-896. DOI: 10.1109/LED.2014.2336592

[69] Kurimoto H, Shibata K, Kimura C, Aoki H, Sugino T. Thermal oxidation temperature dependence of 4H-SiC MOS interface. Applied Surface Science. 2006;**253**(5):2416-2420. DOI: 10.1016/j.apsusc.2006.04.054

[70] Thomas SM, Sharma YK, Crouch MA, Fisher CA, Perez-Tomas A, Jennings MR, et al. Enhanced field effect mobility on 4H-SiC by oxidation at 1500°C. IEEE Journal of the Electron Devices Society. 2014;**2**(5):114-117. DOI: 10.1109/JEDS.2014.2330737